HUNTRON TRACKER

Aplications guide

gate 1 —————— source

gate 2 —————— drain

TESTING A MOS FET
(Metal oxide silicon field-effect transistor)

Sometimes called the "insulated gate FET", the MOS FET is
a high impedance device and requires testing of the sub-
strate bar; between the gates, source and drain; and be-
tween the gates. It will also be necessary to test the
substrate for leakage.

TEST PROCEDURE

TEST POINTS	IMPEDANCE RANGE	ACCEPTABLE RESPONSE
SOURCE TO DRAIN	LOW	
SOURCE TO GATE 1	HIGH	
SOURCE TO GATE 2	HIGH	
DRAIN TO GATE 1	HIGH	
DRAIN TO GATE 2	HIGH	
GATE 1 TO GATE 2	HIGH	

MOS FET's MAY BE CHECKED IN OR OUT OF CIRCUIT

BUT.....they are tested in-circuit with greater ease since
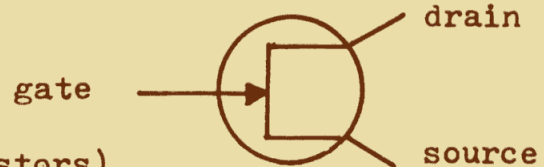the out-of-circuit protective precautions are extensive.

probing

HUNTRON TRACKER

Applications guide

TESTING J-FET's
(Junction field-effect transistors)

gate → drain / source

The construction of a J-FET differs from a Bi-polar in
that two of the contacts are connected to a common sub-
strate bar. Two unique problems occur with J-FET's that
can be difficult, even impossible, to check with other
test instruments.

1.   DECAY OF THE GATE JUNCTION- This does not render
     the device in-operative, but unlike other solid
     state devices, the amount of gain will DECREASE
     as the condition worsens.

2.   LEAKAGE IN THE SUBSTRATE ELEMENT- This can also
     cause DECREASED gain in the device and/or intro-
     duce noise into the circuit.

TESTING J-FET's IN OR OUT OF CIRCUIT

1.   With TRACKER set to the MEDIUM position, place
     one MICROPROBE on the SOURCE and the other on
     DRAIN. A good J-FET will begin with a typical
     two junction display on the scope.

          example:

     This pattern may hold or it may COLLAPSE TO A
     STRAIGHT VERTICAL LINE, depending upon the im-
     pedance of the substrate bar. A LOOP at either
     end of the pattern or vertical lines is also a
     normal condition.

          example:

     This only indicates the CAPACITANCE of the sub-
     strate material. A defective J-FET may display:
          a.   Rounded corners
          b.   Failure to take a substrate charge
               when test probes are first set.

2.   With MICROPROBES gate-to-source a sharp angle
     should be displayed. An identical display should
     be obtained by moving the source lead to drain.
     Any rounding indicates leakage or decay and a
     defective device.

                         good   defective